Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming a semiconductor structure, the method comprising:

forming a patterned oxide layer over a substrate;

forming a USG layer on the patterned oxide layer and exposed portions of the substrate;

forming a BPSG layer on the USG layer;

forming a PE-TEOS layer over the BPSG layer; and

planarizing the PE-TEOS layer such that a portion of the BPSG layer is exposed ~~to form a pre-metal dielectric stack~~;

depositing a metal layer that is above the PE-TEOS and BPSG layers.

2. (Original) The method of claim 1 wherein the planarizing is accomplished by a chemical-mechanical polishing technique.

3. (Currently Amended) The method of claim 1, further comprising forming a TEOS layer on the planarized PE-TEOS layer prior to forming the metal layer and contacting the portion of the BPSG layer.

4. (Original) The method of claim 1 wherein the BPSG layer is between approximately 2k to 8k angstroms thick.

5. (Original) The method of claim 1 wherein the USG layer is between approximately 1k to 4k angstroms thick.

6. (Original) The method of claim 1 wherein a total thickness of the oxide layer, the USG layer, the BPSG layer, and the planarized PE-TEOS layer is less than approximately 15k angstroms.

7. (Original) The method of claim 3 wherein the TEOS layer is between approximately 1k to 5k angstroms thick.

8. (Currently Amended) The method of claim 1, further comprising forming a PE-TEOS layer on the planarized PE-TEOS layer and contacting the portion of the BPSG layer.

9. (Original) The method of claim 8 wherein the PE-TEOS layer is between approximately 1k to 5k angstroms thick.

10. (New) A method of forming a pre-metal dielectric stack on a substrate having active regions formed thereon, comprising:

forming a first layer of undoped silicon-based dielectric material on the substrate;

forming a second layer of doped silicon-based dielectric material on the first layer;

forming a third layer of silicon-based dielectric material on the second layer; and

planarizing the third layer to a degree that a portion of the second layer is exposed.

11. (New) The method of claim 10, comprising forming a fourth layer of silicon-based dielectric material on the third layer and in contact with the exposed portion of the second layer.

12. (New) The method of claim 11 wherein the silicon-based dielectric material of the fourth layer is tetraethyl orthosilicate.

13. (New) The method of claim 11 wherein the silicon-based dielectric material of the fourth layer is plasma-enhanced tetraethyl orthosilicate.

14. (New) The method of claim 10 wherein the silicon-based dielectric materials of the first and second layers are undoped and doped silicate glass, respectively.

15. (New) The method of claim 10 wherein the silicon-based dielectric material of the second layer is borosilicate glass.

16. (New) The method of claim 10 wherein the silicon-based dielectric material of the second layer is borophosphorous silicate glass.

17. (New) The method of claim 10 wherein the silicon-based dielectric material of the third layer is tetraethyl orthosilicate.

18. (New) The method of claim 10 wherein the silicon-based dielectric material of the third layer is plasma-enhanced tetraethyl orthosilicate.

19. (New) The method of claim 10 wherein the planarizing step is performed by chemical-mechanical polishing.

Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1-6. These sheets, which include Figs. 1-6, replace the original sheets including Figs. 1-6.

Attachment: Two replacement Sheets